Appl. No. 09/802,289
Amdt. dated May 4, 2005
Reply to Office Action of March 8, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A processing core comprising:

one or more processing pipelines having a total of N-number of processing paths, each of said processing paths for processing instructions on M-bit data words; and

a plurality of register files, each having Q-number of registers, said Q-number of registers being M-bits wide;

wherein said Q-number of registers within each of said plurality of register files are both private and global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said plurality of register files, said valuc is propagated to a corresponding global register in the other of said plurality of register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said plurality of register files, said value is not propagated to a corresponding register in the other of said plurality of register files, **wherein each of said Q-number of registers is bi-modal to programmably operate in both private and global modes**.

2. (Currently Amended) The processing core as recited in claim 1, wherein **for even values of N that are greater than one,** every two of said N-number of processing paths share one of said plurality of register files.

3. (Original) The processing core as recited in claim 1, wherein a processing instruction comprises N-number of P-bit instructions appended together to form a very long instruction word (VLIW), and said N-number of processing paths process N-number of P-bit instructions in parallel.

4. (Original) The processor chip as recited in claim 3, wherein M=64, Q=64, and P=32.

5. (Original) The processing core as recited in claim 1, wherein said processing pipeline comprises an execute stage which includes an execute unit for each of said N-number of M-bit processing paths, each of said execute units comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.

6. (Original) The processing core as recited in claim 5, wherein an integer processing unit and a floating point processing unit share one of said plurality of register files.

7. (Original) The processing core as recited in claim 1, wherein Q=64, and a 64-bit special register stores bits indicating whether a register in a register file is a private register or a global register, each bit in the 64-bit special register corresponding to one of said registers in said register file.

8. (Original) The processing core as recited in claim 1, wherein each of said plurality of register files is connected to a bus, and a value written to a global register in one of said plurality of register files is propagated to a corresponding global register in the other of said plurality of register files across said bus.

9. (Original) The processing core as recited in claim 1, wherein said plurality of register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.

10. (Currently Amended) A VLIW processing core comprising:

one or more processing pipelines each including a fetch stage, a decode stage, an execute stage, and a write-back stage, said execute stage having an execute unit comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, ~~and~~ **or** said floating point processing units; and

a register file for each of said one or more processing pipelines;

wherein:

an integer processing unit and a floating point processing unit within said one or more processing pipelines both access said register file,

the register file is comprised of Q-number of registers,

said Q-number of registers comprise both private and global registers, **whereby each of said Q-number of registers is dynamically configurable to operate in both private and global modes**,

when a value is written to **a** one of said Q-number of said registers that is ~~a~~ **configured to** global register **mode** within one of said plurality of register files, said value is propagated to a corresponding global register in another register file within the VLIW processing core, and

when a value is written to **the** one of said Q-number of said registers that is ~~a~~ **configured to** private register **mode** within one of said plurality of register files, said value is not propagated to a corresponding register in another register file within the VLIW processing core.

11. (Currently Amended) In a computer system, a scalable computer processing architecture, comprising:

one or more processor chips, each comprising:

a processing core, including:

a processing pipeline having N-number of processing paths, each of said processing paths for processing instructions on M-bit data words; and

a plurality of register files, each having Q-number of registers, said Q-number of registers being M-bits wide;

an I/O link configured to communicate with other of said one or more processor chips, **if more than one,** or with I/O devices;

a communication controller in electrical communication with said processing core and said I/O link;

said communication controller for controlling the exchange of data between a first one of said one or more processor chips and said other of said one or more processor chips;

wherein:

said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween,

said Q-number of registers within each of said plurality of register files comprise both private and global registers, **whereby each of said Q-number of registers is bi-modal to switch between private and global modes,**

when a value is written to **a** one of said Q-number of said registers which is **a switched to** global register **mode** within one of said plurality of register files, said value is propagated to a corresponding global register in the other of said plurality of register files, and

when a value is written to **the** one of said Q-number of said registers which is **a switched to** private register **mode** within one of said plurality of register files, said value is not propagated to a corresponding register in the other of said plurality of register files.

12. (Currently Amended) The computer processing architecture as recited in claim 11, wherein in said processing core of each of said processor chips, **for even**

values of N that are greater than one, every two of said N-number of processing paths share one of said plurality of register files.

13. (Original) The computer processing architecture as recited in claim 11, wherein a processing instruction comprises N-number of P-bit instructions appended together to form a very long instruction word (VLIW), and said N-number of processing paths process N-number of P-bit instructions in parallel.

14. (Original) The computer processing architecture as recited in claim 13, wherein M=64, Q=64, and P=32.

15. (Original) The computer processing architecture as recited in claim 11, wherein said processing pipeline comprises an execute stage which includes an execute unit for each of said N-number of M-bit processing paths, each of said execute units comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.

16. (Original) The computer processing architecture as recited in claim 15, wherein an integer processing unit and a floating point processing unit share one of said plurality of register files.

17. (Canceled)

18. (Previously Presented) The computer processing architecture as recited in claim 11, wherein Q=64, and a 64-bit special register stores bits indicating whether a register in a register file is a private register or a global register, each bit in the 64-bit special register corresponding to one of said registers in said register file.

19. (Previously Presented) The computer processing architecture as recited in claim 11, wherein each of said plurality of register files is connected to a bus, and a

value written to a global register in one of said plurality of register files is propagated to a corresponding global register in the other of said plurality of register files across said bus.

20. (Original) The computer processing architecture as recited in claim 19, wherein said plurality of register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.

21. (Previously Presented) The processing core as recited in claim 1, wherein said Q-number of registers within each of said plurality of register files can switch between being either private or global registers.